REMARKS

Claims 1, 12, 21 and 32 have been amended. Claims 1-9, 12-14, 17-26, 29-34 and 37-39 remain pending in the application. Reconsideration is respectfully requested in light of the following remarks.

Section 103(a) Rejection:

The Examiner rejected claims 1-6, 12-14, 20-26 and 32-34 under 35 U.S.C. § 103(a) as being unpatentable over Saito (U.S. Patent 6,694,475) in view of Bains (U.S. Patent 5,701,438), and claims 7, 17, 29 and 37 as being unpatentable over Saito in view of Bains and in further view of Elliott et al. (U.S. Patent 5,392,425) (hereinafter "Elliott"). Applicant respectfully traverses these rejections in light of the following remarks.

In regard to claim 1, the cited art does not teach or suggest that the second operand is provided by a source other than the first and second memory banks, wherein the source of the second operand and the accumulator memory each comprise a same type and speed of single-ported memory. As discussed in the Background section of the present application, systems that perform block operations, such as parity calculations in storage systems, typically use high speed or dual-ported memory for one operand. The parity generator in Saito is an example of such a system that uses a dual port memory as an operand source to its parity generator. In contrast, Applicant's claimed invention pertains to an apparatus that allows single-ported memory of the same type and speed to be used for an operand source and accumulator. Unlike Applicant's claimed invention, in Saito one operand is provided by either RAM(p1) 30 or RAM(p2) 31, and the second operand is provided by dual-port DRAM 12 (Saito -- col. 9, lines 14-51). RAM(p1) 30 and RAM(p2) 31 are single port memories whereas DRAM 12 is a dual-port memory (Saito -- col. 6, lines 11-18). Saito requires that memory 12 be a dual-port memory in order to store data from both disk 17 (RAM port) and the host

(SAM port). *See* Saito -- Figs. 1 and 3, and col. 6, lines 11-18. Thus, Saito does not teach or suggest that the operands are provided by the same type of single-ported memory.

The Examiner also cites Bains. However, Bains teaches the use of different memory types and speeds (EDO DRAM, SDRAM, FP DRAM in Fig. 2). Thus, Bains actually suggests the desirability of using different memory types and speeds, not the same memory type and speed. The Examiner asserts that col. 7, lines 35-46, suggests using the same type and speed of memory for the source memory and accumulator memory for the parity generator of Saito. However, the Examiner's interpretation of Bains is incorrect. Column 7, lines 35-46, of Bains states as follows:

> In embodiments in which the access speed of each of the memory units is determined, the invention operates to arrange memory units in performance order from highest performance memory device type, highest access speed memory unit, to lowest performance, lowest access speed memory unit. In this case, the order of the memory units 230 and 233 in the address range is determined by their access speed if they are of the same memory type. If the access speed of the devices in both memory units 230 and 233 are the same, then either memory unit may follow memory unit 231 including SDRAM in the main memory 109 address range.

The memory devices discussed in this portion of Bains are all part of the main memory 109 in Bains' system. Thus, Bains' teachings only apply to the configuration of the main memory in a computer system, not to a source memory and accumulator memory for a parity generator as in Saito. The Examiner's cited portion of Bains is in no way suggestive of using the same type and speed of single-ported memory for an operand source memory and accumulator memory of the parity generator in Saito.

The Examiner also asserts that col. 1, lines 11-17, of Bains discloses that a person of ordinary skill in the art would have been motivated to have the source and the accumulator memory each comprise a same type and speed of memory because the data can be accessed at the same rate so as not to reduce the overall performance of the computer system. The Examiner has completely misrepresented the teachings of Bains. Column 1, lines 11-17, of Bains states as follows:

> Memory device speed has not increased as rapidly as microprocessor speed. Thus, memory subsystem performance is often the limiting factor in terms of overall computer system performance. For this reason, it is important to optimize memory subsystem performance in order to take advantage of the power and speed of the microprocessor.

Clearly, this portion of Bains has absolutely nothing to do with the source and accumulator memory architecture of a parity generator. Nor does this portion or any other portion of Bains suggest anything in regard to using the same type and speed of memory for an operand source memory and accumulator memory. To the contrary, Bains' teachings pertain to the use of different types and speeds of memory for the main memory of a computer system.

Furthermore, Saito requires that memory 12 be a dual-port memory in order to store data from both disk 17 (RAM port) and the host (SAM port). *See* Saito -- Figs. 1 and 3, and col. 6, lines 11-18. Thus, it would be counter to Saito's intended purpose to change the dual port memory to a single-ported memory. If a proposed modification would render the prior art feature unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900 (Fed. Cir. 1984). The combination of Saito and Bains actually teaches away from the operands being provided by the same type of memory, given that Bains expressly teaches the desirability of the use of different memory types and speeds and Saito requires that its memory 12 be a dual-port memory.

Similar arguments apply in regard to independent claims 12, 21 and 32.

Allowed Claims:

Claims 8, 9, 18, 19, 30, 31, 38 and 39 have been allowed by the Examiner.

Information Disclosure Statement:

Applicant notes that an information disclosure statement with accompanying Form PTO-1449 was submitted on January 22, 2002, respectively. Applicant requests the Examiner to carefully consider the listed references and return copies of the signed and initialed Form PTO-1449 from this statement. A copy of the previously submitted form PTO-1449 from this information disclosure statement is provided herewith for the Examiner's convenience.

CONCLUSION

Applicants submit the application is in condition for allowance, and notice to that effect is respectfully requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5181-82000/RCK.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

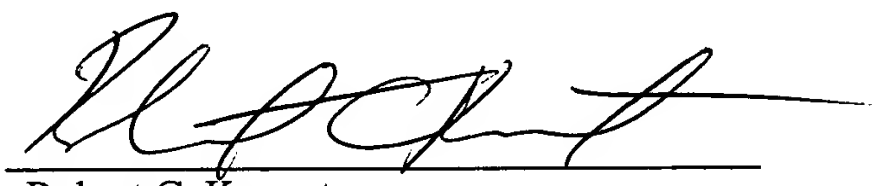
☒ Copy of the previously submitted form PTO-1449 from IDS of Jan. 22, 2002

☐ Notice of Change of Address

☐ Fee Authorization Form authorizing a deposit account debit in the amount of $ for fees ( ).

☐ Other:

Respectfully submitted,



Robert C. Kowert
Reg. No. 39,255
ATTORNEY FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8850

Date: February 7, 2005